**THE CLAIMS IN THE APPLICATION ARE AS STATED BELOW:**

1. (Currently Amended) A digital level shift circuit for providing level shifted output signals in response to input pulses defined by a first transition between a first voltage and a second voltage, and a second transition between the second voltage and the first voltage, the circuit comprising:

a level shifting device that is turned on in response to the first input transition to make an output transition; and

feedback circuitry that obtains a feedback signal indicating that the level shifting device has made the output transition and that turns off the level shifting device during the interval between the first and second input transitions in response to the feedback signal.

2. (Original) The digital level shift circuit of claim 1 in which the level shifting device receives a turn-on signal that turns on the device to make the output transition.

3 (Original) The digital level shift circuit of claim 1 in which the output signal voltage range extends from an offset voltage to an upper voltage that is the sum of the offset voltage and a fixed supply voltage; the offset voltage changing rapidly.

4. (Original) The digital level shift circuit of claim 1 in which the feedback circuitry includes a feedback device, the feedback device providing the feedback signal by turning on when the level shifting device makes the output transition.

5. (Original) The digital level shift circuit of claim 4 in which one of the level shifting device and the feedback device is an n-channel device and the other is a p-channel device.

6. (Original) The digital level shift circuit of claim 5 in which the n-channel and p-channel devices are high voltage MOS transistors.

7. (Original) A digital level shift circuit for providing level shifted output signals, the circuit comprising:

first and second n-channel devices that make output transitions in response to turn-on signals; each turn-on signal turning on one of the n-channel devices to make an output transition; the first and second n-channel devices not receiving concurrent turn-on signals;

first and second p-channel devices that make output transitions in response to turn-on signals; each turn-on signal turning on one of the p-channel devices to make an output transition; the first and second p-channel devices not receiving concurrent turn-on signals; and

sense/prevent circuitry that senses when current greater than a threshold flows through both of the first and second devices of one channel type and, in response, prevents output transitions from being made.

8. (Original) The digital level shift circuit of claim 7 in which the n-channel and p-channel devices are high voltage MOS transistors.

9. (Original) The digital level shift device of claim 7 in which the sense/prevent circuitry prevents output transitions by preventing the first and second devices of the other channel type from receiving turn-on signals.

10. (Original) The digital level shift circuit of claim 7 in which each of the devices of one channel type has a series resistance, each device and its series resistance being connected in series between an output signal line and a common voltage; the sense/prevent circuitry including sensing logic that receives voltages from first and second nodes and that can provide a prevent signal to prevent output transitions from being made; the first node being between the first device and its series resistance and the second node being between the second device and its series resistance, the sensing logic providing the prevent signal only when the voltages at the first and second nodes indicate that current is flowing through the series resistances of both the first and second devices.

11. (Original) The digital level shift circuit of claim 10 in which the sense/prevent circuitry further includes prevent logic that receives the prevent signal and, in response, prevents the first and second devices of the other channel type from receiving turn-on signals.

12. (Original) The digital level shift circuit of claim 11 in which the sensing logic includes an AND gate connected to receive the voltages at the first and second nodes and an inverter on the output of the AND gate and in which the prevent logic includes first and second AND gates each connected to receive the prevent signal from the inverter, the first AND gate also receiving the turn-on signals for the first device of the other channel type and the second AND gate also receiving the turn-on signals for the second device of the other channel type.

13. (Original) The digital level shift circuit of claim 11 in which the sensing logic includes a NAND gate connected to receive the voltages at the first and second nodes and an AND gate connected to receive the prevent signal from the NAND gate, the AND gate also receiving the turn-on signals for the first device of the other channel type.

14. (Original) A digital level shift circuit for providing level shifted output signals, the circuit comprising:

first and second n-channel devices that make output transitions in response to turn-on signals; each turn-on signal turning on one of the n-channel devices to make an output transition; the first and second n-channel devices not receiving concurrent turn-on signals;

first and second p-channel devices that make output transitions in response to turn-on signals; each turn-on signal turning on one of the p-channel devices to make an output transition; the first and second p-channel devices not receiving concurrent turn-on signals; and

control circuitry that controls when each device receives its turn-on signals; the control circuitry including:

feedback circuitry that obtains a feedback signal for each device indicating that the device has made an output transition and that stops the device's turn-on signal in response to the feedback signal; and

sense/prevent circuitry that senses when current above a threshold flows through both of the first and second devices of one channel type and, in response, prevents output transitions from being made.

15. (Original) The digital level shift circuit of claim 14 in which the n-channel and p-channel devices are high voltage MOS transistors.

16. (Original) The digital level shift circuit of claim 14 in which the sense/prevent circuitry prevents output transitions by delaying the first and second devices of the other channel type from receiving turn-on signals; the sense/prevent circuitry further including, for each device, a storage element that stores the device's turn-on signal until the prevent signal ends and the device's feedback signal is received.

17. (Original) The digital level shift circuit of claim 14 in which the sense/prevent circuitry further includes, for each device, a storage element that stores a transmission pulse to the device until the prevent signal ends and the device's feedback signal is received.

18. (Original) The digital level shift circuit of claim 14 in which the feedback circuitry obtains the feedback signal for each device of one channel type from one of the devices of the other channel type, with none of the devices receiving its feedback signal from a device whose feedback signal it provides.

19. (Original) The digital level shift circuit of claim 18 in which the first n-channel device provides the first p-channel device's feedback signal, the first p-channel device provides the second n-channel device's feedback signal, the second n-channel device provides the second p-channel device's feedback signal, and the second p-channel device provides the first n-channel device's feedback signal.

20. (Original) The digital level shift circuit of claim 18 in which the control circuitry further includes:

feedback detection circuitry for each device to distinguish feedback signals from transmissions.

21. (Original) The digital level shift circuit of claim 17 in which the feedback detection circuitry for a device includes an AND gate that determines whether a signal from another device was received when the other device was receiving a feedback signal in response to a transmission.